Abstract of the Disclosur

There is provided a shift register in which multiple stages are connected one after another to each other, the multiple stages having a first stage in which a start signal is coupled to an input terminal, the shift register sequentially outputting output signals of respective stages. The multiple stages have odd stages for receiving a first clock signal, and even stages for receiving a second clock signal having a phase opposite to the first clock signal. Each of the multiple stages has a pull-up section for providing a corresponding one of the first and second clock signals to an output terminal. A pull-up driving section is connected to an input node of the pull-up section, for turning on the pull-up section in response to a front edge of an input signal and for turning off the pull-up section in response to an output signal of a next stage. A pull-down section provides a first power voltage to the output terminal. A pull-down driving section is connected to an input node of the pull-down section, for turning off the pull-down section in response to a front edge of the input signal and turning on the pull-down section in response to the front edge of the output signal of the next stage.